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EXAMINER	
LI, AIMEE J	
ART UNIT	**PAPER NUMBER**
2183	

DATE MAILED: 09/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/843,178	GOSIOR ET AL.	
	Examiner	Art Unit	
	Aimee J. Li	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-20 have been considered. Claims 1-20 have been amended as per Applicant's request.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: RCE as received on 11 July 2005; Extension of Time for 3 Months as received on 11 July 2005; and Amendment as received on 11 July 2005.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 1-3, 6-7, 9-10, 16 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Parady, U.S. Patent No. 5,933,627 (herein referred to as Parady) in view of Steve Furber's ARM System-on-Chip Architecture Second Edition © 2000 (herein referred to as ARM).

5. Regarding claim 1, Parady has taught a programmable, single-chip embedded processor, comprising:

a. A multiple bit, multithreaded processor core (see Fig.3) comprising a single processor pipeline with four or more stages shared by one or more independent processor threads (see Fig.3 and Col.3 lines 35-43), the number 'n' of said processor threads being equal to or less than the number of pipeline stages (see

Fig.1 and 3 and Col.3 lines 2-9 and 50-56). Here, the functional breakdown are not shown to be explicit stages of operation in the pipeline, but being that the UltraSparc processor of Parady (see Col.2 lines 66-67) is pipelined (see Col.3 lines 35-43), it is inherent that the operations of these units occur in a pipelined fashion and the four threads shown is less than the number of pipeline stages.

b. An logic mechanism engaged with said processor core for executing an instruction set within said processor core (41 of Fig.3),

c. A supervisory control unit (112 of Fig.3), controlled by one or more control threads selected from said processor core threads, for examining said core processor state and for controlling said core processor operation (see Col.3 lines 57-65). Here, the thread switching logic monitors cache misses caused by a thread, and subsequently causes a thread switch. The thread switch is controlled by a current thread which can dictate which thread to switch to (see Col.3 lines 57-65).

d. A memory for storing and executing said instruction set data (see 152 of Fig.5); and

e. Wherein

   i. The processor core can concurrently execute as many as 'n' program threads in parallel (see Fig.3 and Col.3 lines 35-43), with each program thread moving serially through the pipeline (see Fig.3 and Col.3 lines 35-43), and with each program thread being executed at a different pipeline stage at a given time (see Fig.3 and Col.3 lines 35-43); and

ii. The pipeline will complete one one-word instruction per clock cycle (see Fig.3 and Col.3 lines 35-43).

6. Parady has not taught

a. Said supervisory control unit being adapted to allow the one or more control threads to set up the initial state of one or more other threads and to start and stop their operation;

b. Said memory being internally integral to the processor, and comprising a main RAM and a boot ROM; and

c. A peripheral adaptor internally integral to the processor and engaged with said processor core for transmitting input/output signals to and from said processor core.

7. ARM has taught

a. Said supervisory control unit being adapted to allow the one or more control threads to set up the initial state of one or more other threads and to start and stop their operation (ARM page 291);

b. Said memory being internally integral to the processor (ARM page 271), and comprising a main RAM and a boot ROM (ARM pages 20 and 271); and

c. A peripheral adaptor internally integral to the processor and engaged with said processor core for transmitting input/output signals to and from said processor core (ARM pages 216-217).

8. A person of ordinary skill in the art at the time the invention was made, and as taught by ARM, would have recognized that the details of an embedded system such as ARM reduces

power consumption by minimizing off-chip activity, e.g. fewer loads from off-chip memory, and increases parallelism (ARM pages 31-32). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the embedded details of ARM in the device of Parady to reduce power consumption.

9. Regarding claim 2, Parady has taught a system as recited in claim 1, wherein said processor pipeline includes an instruction fetch logic stage (see Col.3 lines 2-9), instruction decode logic stage (14 of Fig.3), multiple port register read stage (48/50 of Fig.3), address mode logic stage (see Col.3 lines 2-9), arithmetic logic unit for arithmetic and address calculations stage (see Col.3 lines 50-56), multiple port memory stage (48/50 ofFig.3), branch/wait logic stage (18 of Fig. 1), and multiple port register write stage (48/50 ofFig.3). Here, the functions are not shown to be explicit stages of operation in the pipeline, but being that the UltraSparc processor of Parady (see Col.2 lines 66-67) is pipelined (see Co1.3 lines 35-43), it is inherent that the operations of these units occur in a pipelined fashion.

10. Regarding claim 3, Parady has taught a system as recited in claim 1, wherein said processor core supports "n" multiple groups of independent threads by replicating said common execution logic and said memory (see Fig.3). Here, n is taken to equal one, and thus Parady has taught one group of four independent threads supported by one replication of the execution logic and memory.

11. Regarding claim 6, Parady has taught a system as recited in claim 1, wherein said instruction set includes a processor instruction for enabling individual threads to determine their thread identity (see Fig.4 and Col.3 line 66 - Col.4line 8). Here, certain instructions can enable a

specific thread upon a thread switch, thus determining the identity of the thread that is desired to be switched to.

12. Regarding claim 7, Parady has taught a system as recited in claim 1, wherein said supervisory control unit (112 offig.3) is capable of examining and interpreting the state of multithread processor core operation for the purpose of starting, stopping, and modifying individual multithread processor operation (see Col.3 lines 57-65). Here, the thread switching logic monitors the processing core for a cache miss, and if it determines there was a cache miss, can stop the current thread and start a new thread (see Col.3 lines 57-65), as well as put the threads into interleaving mode (see Col.4 lines 18-29).

13. Regarding claim 9, Parady has taught a system as recited in claim 1, wherein said supervisory control unit is capable of being accessed and controlled by each of said operating core processor threads by using input/output instructions (see CoL.3 line 57 - Col.4 line 8). Here, each thread can access the thread switching logic by providing it with a thread ID to switch to upon a long-latency operation which is detected by the thread switching logic, the thread ID which can be provided in a load or store (input/output) instruction (see Col 4 lines 5-7).

14. Regarding claim 10, Parady has taught a system as recited in claim 9, wherein said controlling operating processor thread is programmable and comprises any of the available threads (see Col.3 line 57 – Col 4 line 8). Here, any of the four threads can cause a cache miss to be detected by the thread switching logic (see Col.3 lines 57-65), and can further be programmed to include a thread field that tells the thread switching logic which thread to switch to (see Col 4 lines 1-8).

15. Regarding claim 16, Parady has taught a system as recited in claim 1, wherein said memory comprises internal memory for storing and executing core processor code (152 of Fig.5) and external memory engaged with said peripheral adaptor (176/180 ofFig.5).

16. Regarding claim 17, Parady has taught a system as recited in claim 1, wherein said supervisory control unit is configured as a peripheral to said processor core (see Fig.3). Here, the thread switching logic is separate from the core functions of fetch, decode, issue and execute.

17. Claims 4-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Parady, U.S. Patent No. 5,933,627 (herein referred to as Parady) in view of Steve Furber's ARM System-on-Chip Architecture Second Edition © 2000 (herein referred to as ARM), as applied to claim 1 above, and further in view of Dickman et al., U.S. Patent No. 4,556,951 (herein referred to as Dickman).

18. Regarding claim 4, Parady has taught a system as recited in claim 1, but has not explicitly taught wherein the system further comprises a condition code mechanism implemented in said instruction set for detecting specific word data types.

19. However, Dickman has taught a system for detecting specific word data type and setting corresponding condition codes so that conventional program control instructions can be used to control processing, rather than modifying existing control instructions to do so (see Col.2 line 57 - Col.3 line 5). Therefore, one of ordinary skill in the art would have found it obvious to modify the processor of Parady to detect specific types of data words and set their corresponding condition codes so that existing control instructions can be used, thereby creating less work and preserving the previous compatibility of the instruction set.

20. Regarding claim 5, Parady in view of Dickman has taught a system as recited in claim 4, wherein the value of the least significant byte of a word is detected to be within a specific range (see Col.8 line 63 - Col.9 line 12).

21. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Parady, U.S. Patent No. 5,933,627 (herein referred to as Parady) in view of Steve Furber's ARM System-on-Chip Architecture Second Edition © 2000 (herein referred to as ARM), as applied to claim 7 above, and further in view of Miyamoto et al., U.S. Patent No. 6,101,569 (herein referred to as Miyamoto).

22. Regarding claim 8, Parady has taught a system of claim 7, but has not explicitly taught wherein the system further comprises a hardware semaphore vector engaged with said supervisory control unit for controlling multithread access to said peripheral and system memory.

23. However, Miyamoto has taught a semaphore vector (see Cots lines 34-51) which controls multithread access to peripherals and system memory (see Col.4 line 66 - Col.5 line 33) so that data is not inadvertently destroyed by another thread (see Col.1 lines 21-36). Therefore, one of ordinary skill in the art would have found it obvious to modify the processor of Parady to include the use of hardware semaphore vector to control access to peripherals and memory so that inadvertent data destruction does not take place, and thus incorrect operation does not result.

24. Claims 11-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Parady, U.S. Patent No. 5,933,627 (herein referred to as Parady) in view of Steve Furber's ARM System-on-Chip Architecture Second Edition © 2000 (herein referred to as ARM), as applied to claim 9

above, and further in view of Fernando et al., U.S. Patent No. 6,272,616 (herein referred to as Fernando).

25. Regarding claim 11, Parady has taught the system as recited in claim 9 above, but has not explicitly taught wherein said controlling operating core processor thread is capable of reconfiguring the overall thread processing method of operation so that other processing threads can support multiple instruction multiple data processing operations.

26. However, Fernando has taught an instruction that allows current processing threads of execution to switch into a SIMD mode or a MIMD mode (see Col.2 lines 58-63) so that processing performance can be increased for a broad range of software types and requirements (see Col.2 lines 27-32). Therefore, one of ordinary skill in the art would have found it obvious to modify the processor of Parady to allow for an instruction that lets the processing threads switch into MIMD mode in order to improve processing performance for a broad range of software types.

27. Regarding claim 12, Parady has taught the system as recited in claim 9 above, but has not explicitly taught wherein said controlling operating processor thread can reconfigure the overall thread processing method of operation so that other processing threads can support single instruction multiple data processing operations.

28. However, Fernando has taught an instruction that allows current processing threads of execution to switch into a SIMD mode or a MIMD mode (see Col.2 lines 58-63) so that processing perfoIIIance can be increased for a broad range of software types and requirements (see Col.2 lines 27-32). Therefore, one of ordinary skill in the art would have found it obvious to modify the processor of Parady to allow for an instruction that lets the processing threads switch

into SIMD mode in order to improve processing performance for a broad range of software types.

29. Regarding claim 13, Parady has taught the system as recited in claim 9 above, but has not explicitly taught wherein said controlling operating processor thread is capable of reconfiguring the overall thread processing method of operation so that an arbitrary number of processing threads can support simultaneously single instruction multiple data processing operations and multiple instruction multiple data processing operations.

30. However, However, Fernando has taught an instruction that allows current processing threads of execution to switch into a SIMD mode or a MIMD mode (see Col.2 lines 58-63) so that processing performance can be increased for a broad range of software types and requirements (see Col.2 lines 27-32), which allows SIMD and MIMD modes to be concurrently executing (see Col.12 lines 1-5). Therefore, one of ordinary skill in the art would have found it obvious to modify the processor of Parady to allow for the processing threads to simultaneously execute in both SIMD mode and MIMD mode in order to improve processing performance for a broad range of software types.

31. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Parady, U.S. Patent No. 5,933,627 in view of Steve Furber's ARM System-on-Chip Architecture Second Edition © 2000 (herein referred to as ARM), as applied to claim 1 above, and further in view of Bishop et al., U.S. Patent No.5, 784,552 (herein referred to as Bishop).

32. Regarding claim 14, Parady has taught the system as recited in claim 1, but has not explicitly taught wherein said supervisory control unit is operable by a first thread process to

start and stop another thread process and to examine and alter state information in single step and multiple step modes of controlled operation.

33. However, Bishop has taught the execution of an application program under the supervision of a debugging program, the debugging program which halts the application program (see Col.5 lines 11-22) and can examine and alter state information via debugging instruction execution in either single-step or multi-step modes of debugging (see Col.7 lines 13-45) so that an application programmer can more thoroughly test and debug their programs in a controlled testing environment (see Col.1 lines 17-35). One of ordinary skill in the art would have recognized that thoroughly tested and debugged programs are less likely to fail and' provide incorrect results. Therefore, one of ordinary skill in the art would have found it obvious to modify the processor of Parady to allow a debugging program to stop and start another program so that instructions in the other program can be thoroughly tested and debugged in both single-step and multi-step modes of debugging.

34. Claims 15 and 19-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Parady, U.S. Patent No. 5,933,627 in view of Steve Furber's ARM System-on-Chip Architecture Second Edition © 2000 (herein referred to as ARM), as applied to claim 1 above, and further in view of Zammit et al., European Patent Application No. 1091292 (herein referred to as Zammit).

35. Regarding claims 15 and 19-20, Parady has taught a system as recited in claim 1, but has not explicitly taught

a. Wherein the system further comprising an identifying bit pattern embedded in the instruction set (Applicant's claim 15);

b. Wherein said identifying bit pattern is used to identify programming code for code protection purposes (Applicant's claim 19); and

c. Wherein said identifying bit pattern does not affect the operation of the instruction execution logic mechanism (Applicant's claim 20).

36. However, Zammit has taught a processor which identifies values in unused bit fields of instruction during a conversion so that the unused bit fields which contain inappropriate values, which could result in incorrect translation, can be corrected before being executed (see p.3 lines 9-16, 35-39). This bit pattern also protects programming code from being incorrectly translated and causing incorrect execution of the program code. This bit pattern also does not affect the instruction execution logic operation, since it is only used to identify whether there are unused bit fields, which contain in appropriate values, and does not cause the execution logic to perform differently from what the instruction intended. Therefore, one of ordinary skill in the art would have found it obvious to modify the processor of Parady to identify values of unused bits so that inappropriate values are not incorrectly translated, and thus incorrect execution does not occur.

37. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Parady, U.S. Patent No. 5,933,627 in view of Steve Furber's ARM System-on-Chip Architecture Second Edition © 2000 (herein referred to as ARM), as applied to claim 1 above, and further in view of Wilske, U.S. Patent No. 4,155,115 (herein referred to as Wilske).

38. Regarding claim 18, Parady has taught a system as recited in claim 1, but has not explicitly taught wherein said peripheral adaptor is capable of controlling analog and digital processing functions.

39. However, Wilske has taught a microprocessor system which has a peripheral controller capable of receiving and controlling inputs from both analog and digital sources (see Col.2 lines 7-34) so that both types of sources can be controlled from one location in order to reduce cost and lessen hardware (see Col.1lines 14-24). Therefore, one of ordinary skill in the art would have found it obvious to modify the processor of Parady to allow its peripheral adapter to control both analog and digital sources so that the amount of hardware needed to control both types of sources can be reduced, thus lowering cost.

Response to Arguments

40. Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

41. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J. Li whose telephone number is (571) 272-4169. The examiner can normally be reached on M-T 7:30am-5:00pm.

42. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

43. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AJL
Aimee J. Li
16 September 2005

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